A Process For Fabricating Oxides

Cross-Reference To Related Application

This present application claims priority from Provisional Application Serial No. 60/140 969 ~~60/140,999~~ (filed June 24, 1999).

Field of the Invention

This present application relates to integrated circuit fabrication and particularly to a technique for fabricating a high quality, planar and substantially stress-free oxide.

Background of the Invention

As integrated circuit (IC) complexity increases, the size of devices within the IC must decrease. To decrease the size of a device, the various elements of a device must be reduced proportionately. This is known as device scaling. In one type of device, a metal-oxide-semiconductor (MOS) structure, device scaling requires that the oxide layer be made thinner. Unfortunately, as conventional oxides are made thinner (scaled), their quality tends to degrade. The degradation in oxide quality tends to adversely impact the reliability of a device using the oxide.

In addition to oxide quality, the reliability of the dielectric material in a MOS structure may be affected by oxide stress and the planarity of the oxide-substrate interface. Oxide stress can result from lattice mismatch and growth induced stress. Lattice mismatch is difficult to overcome and growth stress has been addressed in a variety of ways with mixed results. Stress in the oxide may lead to dislocations and defects especially in the interfacial region. This may result in mass transport paths and leakage current.

The reliability of a device is characterized by a few conventional criteria. For example, in a MOS transistor reliability may be characterized in terms of the change in conventional device parameters over time (known as device parameter drift). Additionally, time-dependent dielectric breakdown (TDDB) may be used to characterize

reliability of the transistor.

Under operating bias (applied voltage) and temperature conditions, device parameters such as threshold voltage (V_t), saturation current (I_{DSAT}) and transconductance (g_m) tend to drift to unacceptable values. In fact, the drift in device parameters during normal operation is thought to be more problematic than other known reliability problems, such as dielectric breakdown of the oxide. Accordingly, in some cases, device parameter drift can cause a device to fail well before dielectric breakdown occurs.

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In order to address the reliability issues discussed above, a variety of approaches have been tried. For example, it is known that the best oxides for many IC devices are grown rather than deposited oxides. Furthermore, the higher growth temperatures may yield a better quality oxide. Unfortunately, there are problems associated with fabricating oxides at high temperatures by conventional techniques. For example, in achieving the high temperatures required in the high temperature oxide growth sequence, the overall thickness of the oxide grown tends to increase. As a result the oxide may be too thick for a reduced dimension device. Thus, in the effort to fabricate a better quality oxide, device scaling objectives may be defeated. Moreover, when cooling down from the high growth temperatures, the viscosity of the grown oxide increases and growth induced stress may result. Given these issues, it is customary in the semiconductor industry to grow oxides at a low temperatures. The drawback to this practice is that by growing oxide at lower temperatures, the oxide quality may be compromised. This reduction in quality adversely impacts reliability of the oxide for reasons discussed above.

What is needed, therefore, is a process for fabricating ultra-thin oxides which overcomes the problems described above.

Summary of the Invention

The present invention relates to a process for fabricating an oxide. A first oxide portion is formed over a substrate at a first temperature below a threshold temperature. A second oxide portion is formed under the first oxide portion at a temperature above the threshold temperature. In an illustrative embodiment, the substrate is oxidizable silicon and the threshold temperature is the viscoelastic temperature of silicon dioxide. The resulting oxide has a low defect density (D_0), a low interface trap density (N_{it}) and the oxide/substrate interface is planar and substantially stress-free.

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Brief Description of the Drawing

The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that in accordance with standard practice in the semiconductor industry the various features are not necessarily drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or decreased for clarity of discussion.

Figure 1a is a schematic cross-sectional view of an exemplary MOS structure according to the present invention.

Figure 1b is schematic cross sectional view of an exemplary MOS transistor according to the present invention.

Figure 2a is a flow chart of an exemplary fabrication sequence in accordance with the present invention.

Figure 2b is a graph of temperature vs. time in accordance with an exemplary fabrication sequence of the present invention.

Figures 3-5 are schematic cross sectional views illustrating the processing sequence of forming the oxide layer in accordance with an exemplary embodiment of the present invention.

Figure 6 is a transmission electron microscope (TEM) lattice image of a conventional oxide on a substrate having a conductive layer on the oxide.

Figure 7 is a transmission electron microscope (TEM) lattice image of an oxide layer on a substrate including a conductive layer on the oxide in accordance with an exemplary embodiment of the present invention.

Figure 8 is a graph of percent degradation of V_T (V_T drift) over time of illustrative oxides of the present invention and a conventional oxide.

Figure 9 is a graph including plots of time vs. substrate current (I_{sub}) indicative of hot carrier aging (HCA) for a conventional oxide and an oxide layer in accordance with an exemplary embodiment of the present invention.

Figure 10 is a graph including plots of mean time to failure (MTTF) vs. electric field for conventional oxide layers and oxide layers in accordance with an exemplary embodiment of the present invention.

Figure 11 is a comparative graph including plots of transconductance (g_m) vs. gate-source voltage (V_{gs}) for 15 x 15 μm^2 NMOSFETs incorporating conventional gate oxide layers and those incorporating gate oxide layers in accordance with an exemplary embodiment of the present invention.

Figure 12 is a comparative graph including plots of drain currents (I_d) vs. drain voltage (V_d) for a 15 x 15 μm^2 NMOSFETs incorporating conventional gate oxide layers and those incorporating gate oxide layers in accordance with an exemplary embodiment of the present invention.

Figure 13 is a comparative graph including plots of cumulative probability vs. leakage for 15 x 15 μm^2 FETS in a n-type tub including conventional gate oxide layers and gate oxide layers in accordance with an exemplary embodiment of the present invention.

Figure 14 is a comparative graph including plots of cumulative probability vs. leakage for 15 x 15 μm^2 FETS in a p-type tub including conventional gate oxide layers and gate oxide layers in accordance with an exemplary embodiment of the present invention.

Detailed Description

The present invention will now be described more fully with reference to the accompanying drawing figures, in which exemplary embodiments of the present invention are shown. Referring initially to Figure 2a, an exemplary sequence for fabricating an oxide layer according to the present invention is shown. Step I includes a relatively rapid temperature increase followed by a more gradual temperature increase. Step I occurs in a dilute oxygen ambient so that very little oxide is grown in this step. Section II includes a low temperature oxide growth step. This results in the formation of a first oxide portion over a substrate at a temperature below a threshold temperature. Step III includes a temperature increase, illustratively in two stages, to a temperature above the threshold temperature. The two stage temperature increase is believed to reduce growth induced stress in the oxide. This two stage temperature increase is followed by a high

temperature oxide growth at a temperature above the threshold temperature. This results in the formation of a second oxide portion below the first oxide portion. An illustrative cooling step is carried out in step IV. This step includes a gradual decrease in the temperature to below the threshold temperature, followed by a more rapid temperature decrease. In this cooling phase, the first oxide portion is believed to act as a sink for stress relaxation.

A characteristic of the present invention is that the interface between the second oxide portion and the substrate is substantially planar. This planarity is generally measured in terms of surface roughness. In the oxide of the present invention the interface has a surface roughness of approximately 0.3nm or less. Moreover, the interface between the substrate and the second oxide portion is substantially stress-free, having on the order of 0 to 2×10^9 dynes/cm^2 of compression. This results in a defect density (D_0) on the order of 0.1 defects/cm^2 or less. Finally, the second oxide portion is believed to be a more dense layer of oxide, when compared to conventional oxides. As a result of the dense and substantially stress free characteristics of the oxide, the interface trap density (N_{it}) of the oxide of the present invention is on the order of 5×10^{10}/cm^2 to 3×10^9/cm^2 or less.

The resultant ultra-thin oxide having improved planarity, being substantially stress free and being more dense has clear advantages over conventional oxides. These advantages include improvements in both reliability and performance in devices incorporating the oxide of the present invention. To this end, deleterious effects of device parameter drift, and time dependent dielectric breakdown (TDDB) are reduced by virtue of the present invention. Moreover, device performance may be improved through reduced leakage current and increased mobility, for example. These characteristics of the oxide of the present invention and the improvements in reliability and performance are discussed more fully herein

Referring to Fig. 1a, an oxide layer 30 in accordance with an exemplary embodiment of the present invention is first described. Illustratively, the oxide layer 30 is incorporated into an integrated circuit. The oxide layer 30 is disposed over a substrate 22, and includes a first oxide portion 31 and a second oxide portion 32. The second oxide portion 32 forms an interface 34 with the substrate 22. The substrate 22 is illustratively silicon; it may be monocrystalline or polycrystalline silicon. Most generally it is oxidizable silicon. Illustratively, the oxide layer 30 has a thickness of approximately 40 Å or less. It is anticipated that the thickness of the oxide layer 30 may be 15 Å - 20 Å;

and may be even less than 15 Å. Moreover, the oxide layer may have a layer of material 33 disposed between it and a conductive layer 26. Layer 33 may be a high-k material, including but not limited to tantalum pentoxide, barium-strontium titanate, and silicate dielectric materials. Additionally, other materials may be disposed between the conductive layer 26 and the oxide layer 30 to achieve a variety of results as would be appreciated by the artisan of ordinary skill.

The exemplary embodiment of Fig. 1a is generally a MOS structure. Clearly a variety of devices and elements may incorporate this structure. These include, but are not limited to a MOS transistor (described below) and a MOS capacitor, a common element in integrated circuits. Still other devices and elements may incorporate the oxide of the present invention, as would be readily apparent to one having ordinary skill in the art to which the present invention relates.

In the exemplary embodiment shown in Fig. 1b, the oxide layer 30 is incorporated into a MOS transistor 21. The MOS transistor includes a source 23 and a drain 24, separated by a channel 25. The transistor may also include lightly doped source and drain regions 27 and 28, respectively. The source, drain and channel may be fabricated by a variety of conventional techniques to form a variety of transistor structures including but not limited to PMOS, NMOS complementary MOS (CMOS) and laterally diffused MOS (LDMOS) devices.

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Turning to Fig. 2b, an illustrative sequence for fabricating the oxide layer 30 by fast thermal processing (FTP) is shown. (Cross sectional views of this exemplary growth sequence and the resulting oxide structure are shown in Figs. 3-5). Segment 20 indicates a wafer boat push step at an initial temperature of approximately 300°C-700 °C, with nitrogen flow of 8.0L/min and 0.02 to 1% ambient oxygen concentration. These parameters are chosen to minimize the growth of native oxide, which can degrade oxide quality as well as consume the allowed oxide thickness determined by scaling parameters (referred to as oxide thickness budget or scaling budget). Additionally, a load lock system or a hydrogen bake, well known to one of ordinary skill in the art, can be used to impede the growth of this undesirable low-temperature oxide.

Segment 21 is a rapid upward temperature increase at approximately 50-125°C per minute to about 750°C –850°C. This step is carried out at a very low oxygen ambient concentration (on the order of 0.05% to 5%) and a high nitrogen ambient. One aspect of the present embodiment relates to the step of upwardly ramping the temperature

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at a relatively high rate (segment 21) to minimize the thickness of the oxide formed in this segment (known as the ramp oxide). This helps control the overall thickness of the oxide 30. Thus, through this step, the desired higher growth temperatures (segments 23 and 26) may be attained without sacrificing the oxide thickness budget. Moreover, this rapid rise in temperature at low ambient oxygen concentrations retards the growth of lower temperature oxide, which may be of inferior quality, as discussed above.

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Segment 22 is a more gradual increase in temperature. Segment 22 proceeds at approximately 10-25°C per minute. In the exemplary embodiment the temperature reached at the end of segment 22 is in the range of approximately 800°C to 900°C. The same oxygen and nitrogen flows/concentrations used in segment 21 are maintained in segment 22. This control of the ramp up in temperature in segment 22 is also important as it helps to prevent overshooting the growth temperature of segment 23. Finally, the low concentration of oxygen in segment 22 selectively retards the growth of oxide during the temperature increase to a higher growth temperature. Again this helps to preserve the oxide thickness budget.

Segment 23 is a low temperature oxide (LTO) growth step. In this step, the ambient oxygen concentration is about 0.1% to about 10% while the ambient nitrogen concentration is 90-99.9%. Dichloroethyline may be added at 0-0.5% for a time that is dependent upon the desired thickness as would be appreciated by one of ordinary skill in the art. At the end of segment 23, an anneal in pure nitrogen may be carried out. In the illustrative sequence of Fig. 2, during segments 20-22 an oxide is grown having a thickness in the range of 5-10 Å. Segment 23 results in the growth of approximately 2.5-10 Å of oxide. Upon completion of segment 23, the growth of the first oxide portion 31 (in Fig. 4) is completed. Illustratively, this first oxide portion is grown at a temperature lower than the viscoelastic temperature of silicon dioxide (T_{ve}), which is approximately 925°C. The first oxide portion 31 may comprise 25-98% of the total thickness of the oxide layer 30. In an exemplary embodiment in which the oxide layer 30 has a thickness of 30 Å or less, the first oxide portion 31 has a thickness of approximately 7.5-20Å. As discussed more fully herein, applicants theorize that the first oxide portion 31 acts as a sink for stress relaxation that occurs during the growth of second oxide portion 32 under first oxide portion 31.

Segment 24 is the first segment in the temperature increase to a temperature above the viscoelastic temperature of silicon dioxide. This ramp up in temperature occurs relatively slowly, at a rate of approximately 5-15°C per minute and in

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a nearly pure nitrogen ambient (the ambient concentration of oxygen in this segment is illustratively 0%-5%). The temperature reached at the end of segment 24 is approximately 50°C below the high temperature oxide (HTO) growth temperature of segment 26. Segment 25 is a modulated heating segment in which the temperature is increased at a rate of approximately 5-10°C per minute to a temperature above the viscoelastic temperature. In the illustrative embodiment the HTO growth temperature is in the range of 925-1100°C. The same flows/concentration of oxygen and nitrogen of segment 24 are used in segment 25. At the end of segment 25, the HTO growth temperture is reached.

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Segments 24 and 25 are useful steps in the of the exemplary embodiment of the present invention. As was the case in the temperature ramp-up to segment 23 (the LTO growth segment) the careful ramp-up of temperature in segments 24 and 25 prevents overshooting the desired growth temperature, in this case the HTO growth temperature of the present invention. The rate of temperature increase at the illustrated low ambient oxygen concentration is useful in retarding oxide growth thereby preserving the oxide thickness budget. Finally, applicants believe that the careful heating in a low oxygen ambient in segments 24 and 25 reduces growth stress, and consequently a reduces the occurrence of oxide growth defects (e.g. slip dislocations and stacking faults).

Segment 26 is the HTO growth step, where the growth temperature is illustratively above the viscoelastic temperature of silicon dioxide. The temperature achieved at the end of segment 25 is maintained in the growth step in segment 26 in a 0 to 25% oxygen ambient for approximately 2 to 20 minutes so that an additional 2-12 Å of oxide may be grown at high temperature. The second portion may comprise on the order of 2-75% of the total thickness of the oxide layer 30. The final portion of segment 26 may include an anneal in pure nitrogen. Applicants believe (again without wishing to bound) that the high temperature growth above the viscoelastic temperature (approximately 925°C) results in the growth of an oxide (second oxide portion 32) having certain properties. For example, it is believed that the second oxide portion 32 is more amorphous, and thereby has little, if any, crystalline structure and short range order. This results in a denser oxide. To this end, the SiO_4 tetrahedron structure connected by O-Si-O chain, (characteristic of silicon dioxide) is more random than in conventional oxides. The random nature of the molecular structure of the second oxide portion 32 results in a more densely packed oxide. Accordingly, as will be appreciated through the discussion herein, the second oxide portion 32 is believed to have shorter Si-O bond length and greater Si-O bond strength when compared to conventionally grown oxide.

Segment 27 of the exemplary embodiment of Fig. 2 is a cooling segment also referred to as a modulated cooling segment. A temperature ramp down is carried out at a rate of approximately 2-5°C per minute to a temperature at the end of segment 27 which is below the viscoelastic temperature. For example, the temperature reached at the end of segment 27 is in the range of 900- 800°C. Segment 27 is carried out in a nearly pure nitrogen ambient, which is inert. During the cooling of a grown oxide to below the viscoelastic temperature, stress may result in the oxide, particularly at the substrate-oxide interface. As a result of this stress, defects such as slip dislocations and oxidation induced stacking faults may be formed at energetically favored sites such as heterogenities and asperities. These defects may be viewed as routes for diffusional mass transport and leakage current paths which can have a deleterious impact on reliability and device performance. The modulated cooling segment, and the stress absorbing or stress sink characteristics of the first oxide portion 31 (particularly during the modulated cooling segment) results in a substantially stress free oxide-substrate interface. Moreover, the defect density is reduced. Finally, segment 28 represents a further ramp down at a faster rate on the order of approximately 35-65°C per minute in an inert ambient such as pure nitrogen. Segment 29 is the boat pull at about 500°C in a pure nitrogen ambient.

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Figs. 3-5 show the cross sectional view of the steps of forming the oxide 30. The substrate 22 is generally oxidizable, illustratively monocrystalline or polycrystalline silicon, or silicon islands in silicon on insulator (SOI) substrates. The first oxide portion 31 may be considered the low temperature oxide (LTO) portion, having been formed below approximately 925°C. In addition to providing a stress sink during the formation of the second oxide portion 32 the first oxide portion 31 enables oxide growth thereunder. As such, first oxide portion 31 must allow the diffusion of oxygen there through so that oxidation of the substrate 22 can occur, resulting in the second oxide portion 32. In the illustrative embodiment, the first portion is silicon dioxide. However, other materials may be used in this capacity as well. Alternative materials include but are not limited to a lightly nitrided (for example 0.2 to 3% nitrogen by weight) silicon dioxide layer so that boron penetration is prevented, which is beneficial in the prevention of poly-depletion. Moreover, the first oxide portion 31 may be steam oxide or a grown-deposited composite oxide layer. The second oxide portion 32 may be considered the high temperature oxide (HTO) portion grown at a temperature above the viscoelastic temperature of 925°C. For purposes of illustration, the high temperature growth of the second portion 32 is in the range 925°C - 1100°C.

Characteristics of the oxide layer 30 of the present invention include improved interfacial planarity and a reduction in the stress both in the bulk of the oxide and at the interface between the oxide and the substrate. This becomes readily apparent from a comparison of the Figures 6 and 7.

Figure 6 is a TEM lattice image of a MOS structure incorporating conventional oxide; Figure 7 is a TEM lattice image a MOS structure incorporating the exemplary oxide of the present invention. Figure 6 shows a substrate 62, a conventional oxide layer 60 and a conductive layer 66. In the image of Fig. 6, there is a stress band 63 (dark contrast) indicating the existence of a strain field between the oxide 60 and the substrate 62. In addition, the interface between the oxide 60 and the substrate 62 is relatively rough (i.e. not planar). Conventional oxides exhibit a surface roughness on the order of 5Å or greater. Among other drawbacks, this degree of roughness can result in carrier scattering in the channel of an exemplary MOS transistor, resulting in reduced carrier mobility.

In contrast to the conventional oxide in Fig. 6, the interface between the graded grown oxide 30 and the substrate 22 in the exemplary embodiment of the present invention shown in Fig. 7 shows no dark contrast in the TEM image. Therefore, there is no noticeable stress band. Instead, the interface between the graded grown oxide 30 and the substrate 22 in the illustrative embodiment is substantially stress free. Moreover, the interface is substantially planar without any observable breakage in the Si (111) lines near the interface. Using standard stress measurement techniques such as x-ray micro-diffraction techniques, the silicon (400) Bragg peak profile indicates 2 x 10^9 dynes/cm^2 of compression by Warren-Averbach analysis. In contrast, conventional oxides exhibit 9 x 10^{10} to 1 x 10^{10} dynes/cm^2 of tension. Furthermore, although not discernable in the TEM of Fig. 7, the bulk oxide is substantially stress free having 0-2 x 10^9 dynes/cm^2 of compression measured by similar technique. Finally, the interface between the oxide 30 and the substrate 22 is substantially planar having a planarity that is not detectable within the resolution of conventional TEM imaging devices (approximately 3Å).

As alluded to above, by virtue of the substantially stress free and planar Si-SiO_2 interface and the denser second oxide portion 32 formed by the present invention oxide of the present invention, there are improvements in the reliability of devices employing the oxide of the present invention. The device parameter drift during normal operation is often more significant than oxide breakdown when evaluating the reliability device employing the thin gate oxide. Device parameter drift can cause a device to fail

the required parameter specifications long before an oxide breakdown event occurs. Drift in devices is dominated by two mechanisms. In a p-MOS device, bias- temperature (BT) drift is the dominant factor, while in an n-MOS device hot carrier degradation (also referred to as hot carrier aging (HCA)) dominates.

The migration to surface channel devices for better off-state leakage performance can result in drift in the threshold voltage (V_T) under bias temperature (BT) conditions. This drift phenomenon is attributed to the creation of hot holes due to impact ionization by electrons which have tunneled into the silicon substrate. These hot holes are trapped within the oxide. It is theorized that the traps within the oxide are due to weak Si-O bonds in the bulk oxide which behave like hole traps. These trapped holes act as positive charge within the oxide resulting in shift in the threshold voltage (V_T). In contrast to conventional oxides, the second oxide portion 32 of the present invention is believed to have a reduced number of weak silicon-oxygen bonds. Accordingly, there is a reduced incidence of traps. Again, this follows from the substantially stress free, dense nature of the second oxide portion 32. The propensity for threshold voltage shift in the oxide of the present invention is significantly lower. This is shown in Fig. 8, where the percentage degradation of threshold voltage in two illustrative samples of the oxide of the present invention having thicknesses of 36 Å (plot 81) and 32 Å (plot 82) is compared to a conventional oxide having a thickness of 33 Å (plot 83). As is clear from Fig. 8, bias temperature (BT) drift is significantly lower in devices using the oxide of the present invention.

Another phenomenon that can adversely impact the reliability of a device is hot carrier aging (HCA). In sub-micron gate structures, hot carrier effects result from a increased lateral electric field in the reduced length channel. This causes inversion-layer charges to be accelerated (or heated) to an extent that they may cause a number of harmful device phenomena, commonly referred to as hot carrier effects. An important hot carrier effect from the standpoint of reliability in devices is the damage inflicted on the gate oxide and/or the silicon-silicon dioxide interface by hot carriers. Hot carrier aging is believed to be due to interface trap generation or the breaking of passivating dangling bonds. To this end, dangling bonds in the silicon-silicon dioxide interface are conventionally passivated in a hydrogen ambient, thereby reducing the number of interface traps. While this passivation technique has met with some success in conventional oxides, hot carriers can readily break silicon-hydrogen bonds, thereby re-establishing the previously passivated interface traps. The traps in the interface act as scattering centers, thereby reducing the mobility of carriers within the channel. As is

known, the drive current, I_{on} (or saturation current, I_{dsat}), and the transconductance g_m are directly proportional to the mobility of the carriers in the channel. Accordingly, as the scattering centers become more abundant due to hot carrier effects, the mobility of carriers in the channel is reduced, and the drive current and transconductance are reduced. Thus, the number of interface traps can cause the device to degrade (age) due to drift in device parameters such as drive current and transconductance. This degradation has a deleterious impact on device reliability.

The oxide of the present invention has a reduced incidence of dangling silicon bonds, and thereby a reduced number of interface traps. Applicants theorize that this is a result of a more complete oxidation process and because the interface is substantially stress-free and planar. Moreover, since there are fewer interface traps in the oxide of the present invention, there are fewer traps passivated with hydrogen; and it is anticipated that there will be less device drift due to hydrogen release in devices which incorporate the oxide of the present invention.

Measured by standard technique, the interface trap density (N_{it}) of the oxide of the present invention is on the order of 3 x 10^9/cm^2 to 5 x 10^{10}/cm^2 or less. The resulting improvement in hot carrier aging can be seen clearly in the graphical representation of Fig. 9. The hot carrier aging criteria by convention is a 15% change in transconductance. The plot labeled 90 is for a device incorporating a 32 Å oxide layer fabricated in accordance with the present invention. The plot labeled 91 is for a device incorporating for a conventional oxide of the same thickness. For example, the substrate current limit of 3 μA/μm is achieved at 120 hours in a conventional oxide in a MOSFET; in an exemplary oxide of the present invention this is limit achieved at 400 hours. As will be readily appreciated of those of ordinary skill in the art, hot carrier aging is improved by a factor of 3-10 by the oxide of the present invention when compared to conventional oxides.

The oxide of the present invention also results in an improvement in the time dependent dielectric breakdown (TDDB), another measure of reliability of the MOS device. This improvement in TDDB is believed to be a direct result of the stress free and high quality silicon-silicon dioxide interface of the present invention. As discussed above, due to the planar and substantially stress free interface between the substrate and oxide, the defect density D_0 is lower. As a result, it is believed that there are fewer defects, which can lead to diffusional mass transport and leakage current. Ultimately this can lead to an improvement in charge fluence or charge –to-breakdown(Q_{bd}) and

dielectric breakdown under temperature (for example >150°C to 210°C) and field acceleration (for example 3-6 MV/cm).

As shown in Fig. 10 the oxide of the present invention results in a factor of 8-10 improvement of TDDB when compared to conventional oxides. In particular the mean time to failure (MTTF) vs. electric field strength is plotted for various conventional oxides and an exemplary oxide of the present invention in a 0.25 microns CMOS device. The plot 100 is for an illustrative oxide of the present invention having a thickness of 32 Å, while the corresponding conventional oxides of the same thickness are represented by plots 102 and 103. For purposes of illustration in an exemplary device, the oxide of the present invention exhibits a breakdown at 10^5 sec at a field of 5.5 MV/cm, compared to the conventional oxide which exhibits a breakdown at approximately 2×10^4 sec at the same electric field. Plot 101 is for an illustrative oxide of the present invention having a thickness of 28 Å, while that of plot 104 is for a 28 Å thick layer of conventional oxide. As can be seen, the illustrative oxide of the present invention exhibits a breakdown at about 2×10^4 sec for a 5.5 MV/cm electric field compared to a breakdown at 7×10^3 sec for the same electric field for a conventional oxide.

As stated previously, device performance is also improved by virtue of the oxide of the present invention. As discussed above, the carrier mobility within the channel can be significantly impacted by the number of traps and the degree of surface roughness (planarity) at the oxide-substrate interface. A more planar (less rough) interface and a reduction in the number of traps is manifest in an improvement in mobility. This results in an improvement in transconductance. This can be seen most readily from a review of Fig. 11. The even number plots 110, 112, 114, 116, 118, show the transconductance vs. gate-source voltage in an illustrative device using the oxide of the present invention. The odd number plots (111, 113, 115, 117 and 119) are plots of tranconductance vs. gate-source voltage in devices using conventional gate oxides. The tranconductance vs. gate-source voltage (V_{gs}) are plotted for a 15 x 15 μm^2 NMOSFET. Plots 110 and 111 are for a drain voltage of 2.1 volts. Plots 112 and 113 are for a drain voltage of 1.6 volts, while plots 114 and 115 are for a drain voltage of 1.1 volts. Plots 116 and 117 are for a drain voltage of 0.6 volts and plots 118 and 119 are for a drain voltage of 0.1 volt. As would be appreciated by one of ordinary skill in the art, Fig. 11 shows the oxide in accordance with exemplary embodiment of the present invention provides a 5-6% increase in channel mobility. This results in an improvement of drive current (saturation current I_{dsat}) on the order of 20% in the illustrative embodiment.

Turning to Fig. 12, a comparative result of the oxide of the present invention and conventional oxides for a drive current for a 15 x 15 μm^2 NMOSFET is shown. The drain current is plotted vs. drain voltage for a series of gate voltages. Plots 120 and 121 are for gate voltages of 2.5 volts for the oxide layer of the present invention and a conventional oxide, respectively. Plots 122 and 123 are for a gate voltage of 0.2 voltages for the oxide of the present invention and a conventional oxide, respectively. Finally, plots 124 and 125 are for a gate voltage of 1.5 volts for the oxide of the present invention and a conventional oxide, respectively. As can be appreciated by one having ordinary skill in the art, devices incorporating the oxide of the present invention show improved sub-threshold and saturation characteristics compared to devices using conventional oxides.

Leakage current characteristics for a transistor employing the oxide of the present invention are also improved. As discussed above, leakage current is believed to be attributable to oxide defects (D_o). The oxide of the present invention has a defect density of 0.1 defects/cm^2 or less. Again, for thin gate dielectrics, the major contributors to D_o are the growth induced defect density and the intrinsic stress within the oxide layer. The defects are formed at energetically favored sites such as heterogenities and asperities. These defects tend to grow outwardly as oxidation consumes silicon around the defect and eventually a network of defects may exist. These defects may be viewed as pipes for diffusional mass transport as well as potential leakage current paths, which can have a significant impact on device reliability and performance.

Figure 13 is a graph of cumulative probability vs. leakage current for gate oxides in an n-type tub at a voltage 2.0 volts. Plot 130 is for a gate oxide layer in accordance with the present invention having a thickness of 28 Å, while plot 131 is for a conventional oxide of the same thickness. Plot 132 is for an oxide layer of the invention of the present disclosure having a thickness of 32 Å, while plot 133 is for a conventional oxide having a thickness of 32 Å.

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Figure 14 presents various leakage plots for a p-type tub at a voltage of 2.0 volts. Plot 134 is for a gate oxide in accordance with the present invention having a thickness of 28 Å, and plot 135 is for a conventional oxide of the same thickness. Plot 137 is for an oxide of invention of the present disclosure having a thickness of 32 Å, while plot 137 is for a conventional oxide layer having a thickness of 32 Å. From Figs. 13 and 14 it can be appreciated that the oxide of the present invention offers a 8-10 times improvement leakage current. Moreover, with this significant improvement in leakage

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current, as one of ordinary skill in the art would readily appreciate, the charge control over the channel is improved, with improved sub-threshold characteristics (I_{off}).

The invention having been described in detail, it is clear that variations and modifications will be apparent to one of ordinary skill in the art. Such modifications and related embodiments of the disclosed invention are included with the scope of the appended claims.